

30. (Previously presented) The method of claim 26, wherein inputting the length of the first instruction comprises inputting said length from the length decoder to the first shifter via an intermediate latch.

31. (Currently amended) Logic for aligning instruction in an instruction stream, the logic comprising:

a first shifter;

a second shifter; and

a length decoder, wherein an output of the first shifter forms a direct input to the second shifter and exclusively defines data to be shifted therein, an output of the second shifter is sent to the length decoder via an intermediate latch, and wherein a length of a current instruction in the length decoder is directly input into the second shifter and the second shifter shifts the data based exclusively on the length of the current instruction, wherein the second shifter has a maximum capacity to shift which is less than the maximum instruction length.

32. (Previously presented) The logic of claim 31, wherein a length of the current instruction in the length decoder is input into the first shifter via an intermediate latch.

33. (Previously presented) The logic of claim 31, wherein the first shifter has a greater shifting capacity than the second shifter.

34. (Previously presented) The logic of claim 31, wherein the second shifter has a capacity of 16 bytes and the second shifter has a capacity of 8 bytes.

35. (Currently amended) Logic for aligning instructions in an instruction stream, the logic comprising:

first shifting means for shifting bytes of the instruction stream;

second shifting means for shifting bytes of the instruction stream; and length decoding means for determining a length of an instruction in the instruction stream, wherein an output of

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